Customer No.: 31561
Application No.: 10/708,371
Docket NO.: 11955-US-PA

REMARKS

Present Status of the Application

Upon entry of the amendments in this response, claims 1-15 are still pending. During this response, a copy of amended specification is respectfully submitted so that the amended specification is free of any minor error. It is believed that no new matter is added by way of amendments made to the specification. For at least the foregoing reason, applicants respectfully submit that claims 1-15 patently define over prior art of record and reconsideration of this application is respectfully requested.

Discussion of Objections to The Claims Under 35 U.S.C. 102(e)

1. *Claims 1-15 are rejected Under 35 U.S.C. 102(e) as being anticipate by U.S. 6,759,906 B2 (Matsunaga et al., hereinafter referred as Matsunaga).*

Regarding to claim 1, Fig.1 of Matsunaga discloses a power amplifier with an active bias circuit (10), comprising: a power transistor (Q1) with a gate connected to a gate bias voltage (Vg1); and an active bias circuit (10) connected to an input power terminal (Vapc) and the gate of the power amplifier transistor (Q1)for receiving an input power from the input power terminal (Vapc) and outputting the gate bias voltage to the gate, wherein the gate bias voltage is increased corresponding to an increase (see Fig.2) of the input power (Vapc). Likewise, objections to the independent claim 1

are also applied to the dependent claims 7 and 13.

In response thereto, applicant respectfully traverses the preceding objections based on the following arguments and withdrawn of the claims 1-15 is respectfully requested. To anticipate the claims, the cited reference, Matsunaga, should teach, suggest or disclose all limitations of the claims. First of all, according the preceding objections, in Matsunaga, Vapc is referred to as an input power terminal. However, from lines 14-15, col. 9, in Matsunaga, there discloses that the voltage Vapc is output from the automatic power control circuit. Also from Fig.23, evidently, the voltage Vapc is used as a bias voltage for biasing a bias control circuit 10. As a result, the input power as claimed in the independent claims 1, 7 and 13 should not be referred as a voltage, "Vapc", disclosed in Matsunaga as alleged by the examiner, rather than "Pin" disclosed in Fig.1 that also is verified by an efficiency equation (i.e. EFF=(Pout – Pin)/ Vdd Id), as disclosed in line 56, col. 10, in Matsunaga.

Accordingly, the examiner's allegation that the gate bias voltage is increased corresponding to an increase (see Fig.2) of the input power (Vapc), is also incorrect because the input power of the present invention is not referred to "Vapc", but to "Pin" as disclosed in Matsunaga. Moreover, Matsunaga does not mention any relationship between the gate bias voltage and the input power of the power amplifier at all. Therefore, Matsunaga fails to teach, suggest or disclose "the gate bias voltage is

increased corresponding to an increase of the input power," as claimed in the independent claims 1, 7 and 13. In other words, the independent claims 1, 7 and 13 are not anticipated by Matsunaga; that is, these independent claims are patentable over Matsunaga under 35 U.S.C. 102(e).

Regarding dependent claims 2-6, 8-12 and 14-15, no matter whether they are conventional, they should be patentable as a matter of law for the reason that they contain all limitations of their corresponding patentable independent claims 1, 7 and 13, respectively.

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CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-15 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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